REMARKS

Applicants respectfully request that the Amendment and Response to Final Office Action be admitted under 37 C.F.R. 1.116. Applicants submit that this amendment presents claims in better form for consideration on appeal. Furthermore, applicants believe that consideration of this amendment could lead to favorable action that would remove one or more issues for appeal. Applicants submit that, thus, there is good and sufficient reason why this amendment should be admitted now. Reconsideration of this application, as amended, is respectfully requested. Claims 1-11, 13-17, and 19-26 are pending. Claims 8-11, 13-17, and 19-26 stand rejected. Claim 13 has been objected to.

Claims 8 and 14 have been amended. Claims 1-7, 12, 16, 18 and 21 – 26 have been cancelled. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Claim Objections

Claim 13 has been objected to because of the following informalities: Claim 13 depends from claim 1 which is a non-elected withdrawn claim.

Applicants have amended claim 13 to properly depend from claim 8.

Rejections Under 35 U.S.C. § 103(a)

Claims 8-9, 11, 13-15, 17,19-22 and 24-26 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Publication No. 2002/0163072 of Gupta, et al. ("Gupta") in view of U.S. Patent Publication No. 2003/0003703 of Barth, et al. ("Barth") and U.S. Patent Publication No. 2003/0053081 of Forouhi, et al. ("Forouhi"). The Examiner has stated that

Gupta discloses a three-dimensional (3-D) integrated chip system, comprising: a first wafer (Figs. 2-10 el. 202) including one or more integrated circuit (IC) devices (el. 112), metallic lines (el. 210) deposited via an interlevel dielectric (ILD) and settled on the surface higher than the ILD (el. 113, 116; Fig. 7) for wafer-to-wafer bonding and electrical interconnection, and an ILD recess surrounding the metallic lines deposited via the ILD (Fig. 7); and a second wafer (el. 100) including one or more integrated circuit (IC) devices (el. 112), metallic lines (el. 132) deposited via an interlevel dielectric (ILD) and settled on the surface higher than the ILD (el. 113, 116; Fig. 7) for wafer-to-wafer bonding and electrical interconnection, and an ILD recess surrounding the metallic lines deposited via the ILD (Fig. 7), wherein the metallic lines on the surface of the second wafer are bonded with the metallic lines on the surface of the first wafer to facilitate direct metal bonding between active IC devices on the adjacent wafers (Fig. 8; p. 3, para. 29-30). Gupta also discloses wherein the metallic lines include Copper (Cu) bonding pads deposited on opposing surface of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers (p. 3 para. 29); wherein the ILD recess is created by selectively etching the ILD surrounding the metallic lines deposited via the ILD (p. 3 para. 29); and wherein the first wafer is thinner than the second wafer to conform to height differences of the metallic lines across opposing surfaces of the adjacent wafers (p. 3 para. 31).

Gupta does not disclose a high temperature deformable interlayer dielectric, or a SiLK dielectric. However, Barth discloses wherein the ILD is a high-temperature deformable dielectric used to allow the bonding areas to be self-leveling to account for height variations across the adjacent wafers to be bonded, and wherein the high-temperature deformable dielectric is SILK which exhibits a glass transition near 450 degrees C while the metallic lines exhibit a bonding temperature of about 400 degrees C (p. 2 para. 18-19). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the SiLK dielectric of Barth with the IC system of Gupta. SiLK dielectric has energy band gaps and extinction coefficients that are sensitive indicators of the curing temperature and time for the curing process (Forouhi – p. 1 para. 10).

(p. 2-4 Office Action 10/7/03)

Applicants respectfully submit that claim 8, as amended, is not rendered obvious by Gupta in view of Barth and Forouhi. Amended claim 8 includes the following limitations.

A three-dimensional (3-D) integrated chip system, comprising:

a first wafer including one or more integrated circuit (IC) devices, a first plurality of metallic bonding pads deposited via an interlevel dielectric (ILD) for wafer-to-wafer bonding and electrical interconnection, the first plurality of metallic bonding pads having a variety of heights, and an ILD recess surrounding the first plurality of metallic bonding pads deposited via the ILD; and

a second wafer including one or more integrated circuit (IC) devices, a second plurality of metallic bonding pads deposited via an interlevel dielectric (ILD) for wafer-to-wafer bonding and electrical interconnection, the second plurality of metallic bonding

pads having a variety of heights, and an ILD recess surrounding the first plurality of metallic bonding pads deposited via the ILD;

wherein the first plurality of metallic bonding pads is bonded to the second plurality of metallic bonding pads to establish electrical connections between active IC devices on the adjacent wafers; and

wherein the ILD is a high-temperature deformable dielectric used to allow the bonding areas to be self-leveling to facilitate the bonding of wafers having bonding pads of a variety of heights.

(Amended claim 8) (Emphasis added)

Applicants have amended claim 8 to include the limitations that the bonding pads are a variety of heights and that the ILD is used to facilitate the bonding of wafers having bonding pads that are a variety of heights. Applicants respectfully submit that none of Gupta, Barth or Forouhi disclose these limitations.

As stated by the Examiner, Gupta does not disclose a high-temperature deformable ILD. While Barth does disclose such an ILD, Barth does not disclose that the ILD is used to "allow the bonding areas to be self-leveling to account for height variations across the adjacent wafers." Barth discloses

> [0018] Turning now to FIGS. 1A-O, there is shown a dual Damascene process flow commonly used for the manufacture of integrated circuits having copper interconnects and low k dielectric layers. The illustrated Damascene process flow is exemplary only. It should be understood that a variety of processes can be used to integrate copper and low k dielectrics into the integrated circuit and the process shown is not intended to be limiting. Other integration processes suitable for use in the present invention will be apparent to those skilled in the art in view of this disclosure.
>
> [0019] The Damascene process is shown occurring on an underlying metal layer generally designated 10 having a completed metal interconnect and dielectric layer. The metal layer is formed from a conductive material such as aluminum, copper, tungsten, an aluminum alloy, a tungsten alloy or a copper alloy. Preferably, the metal interconnect is copper and the dielectric layer is a low k material. Preferably, the low k dielectric layer is a polymeric dielectric known under the trade mark SILK (dielectric constant k=2.65), and commercially available by the Dow Chemical Company. The circuit design for this embodiment comprises a logic, SRAM or DRAM array having one or more redundant segments in a region adjacent to the primary memory array. Elements of the logic, SRAM or DRAM integrated circuit are concurrently formed elsewhere on the wafer. The first step in the fabrication of each copper interconnect level is deposition of a thin dielectric cap layer of silicon nitride or silicon carbide 12 as shown in FIG. 1A. For example, a thin dielectric cap layer suitable for use in the present invention is commercially available from Applied Materials under the the trade name BLOK. The dielectric cap layer acts as a barrier against diffusion of copper between metal levels and also serves as an etch stop

> in a dielectric etch process. In FIG. 1B, deposition of a thick low k dielectric layer 14 immediately follows deposition of the cap and etch stop layer. The low k material may have a thin layer of oxide on an upper surface. The dielectric layer is patterned by conventional photolithographic techniques using a photoresist as a masking material to form the vias 20 as shown in FIG. 1C. The photoresist 16 is coated onto the low k dielectric layer 14, patterned by exposure to activating energy, and subsequently developed to form a relief image. In FIG. 1D, the relief image is then partially etched into the dielectric layer using conventional etching techniques known to those skilled in the art. The photolithographic process is repeated to form a trench layer and subsequently etched as shown in FIGS. 1E-F.

(Barth, page 2, paragraphs 18-19)

None of the cited portion of Barth, nor the remainder of Barth disclose bonding pads having a variety of heights, nor do the figures of Barth disclose such.

Forouhi likewise does not disclose bonding pads having a variety of heights. Forouhi discloses

> [0010] As a way of example, the modifying-process can be a curing process in a thermal-activated polymer film such as a SILK dielectric film, controlled by the curing temperature and the curing time. The energy band-gap E.sub.g and the spectra of extinction coefficient k=k(.lambda.) of a SiLK dielectric film exhibit pronounced changes with the curing temperature and curing time. The spectra of extinction coefficient K appears to be particularly sensitive to the curing temperature and curing time in the wavelength range of 320 -370 nm. As such, the energy band-gap E.sub.g and extinction coefficient K provide sensitive "indicators" of the underlying curing process taking place in a SILK dielectric film.

(Forouhi, page 1, paragraph 10)

None of the cited portion of Forouhi, nor the remainder of Forouhi disclose bonding pads having a variety of heights, nor do the figures of Forouhi disclose such.

For these reasons, applicants respectfully submit that amended claim 8 is not rendered obvious by Gupta in view of Barth and Forouhi. Given that claims 9 – 11 and 13 depend from claim 8, it is respectfully submitted that claims 9 – 11 and 13 are, likewise, not rendered obvious by Gupta in view of Barth and Forouhi.

Claims 10, 16, and 23 stand rejected under 35 U.S.C. § 103 as being unpatentable over Gupta in view of Barth and Forouhi as applied to claims 8-9, 11 and 13-15 above and further in view of U.S. Patent No. 5,656,554 of Desai, et al. ("Desai"). The Examiner has stated that

> Gupta in view of Barth and Forouhi do not disclose wherein the ILD recess is created by a Chemical Mechanical Polish (CMP). However, Desai discloses controlling the solution of a CMP slurry wherein a surrounding dielectric material would be polished or removed at a faster rate than a center conductive/metallic plug (col. 4, lines 9-15, 2038; col. 5, lines 6-15). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the CMP slurry and procedure of Desai with the IC system of Gupta, Barth, and Forouhi in order to avoid overpolishing or dishing a conductive plug surrounded by dielectric material.

(p. 4, Office Action 10/7/03) (Emphasis added)

> Desai discloses
>
> The sacrificial layer may be formed from a wide variety of materials such as silicon dioxide from, for example, chemical vapor deposition; photoresist; polyimide; etc. The desirable characteristics of the sacrificial layer 40 include a relatively low removal rate for the first planarization process, and a relatively high removal rate for the second planarization process.

(Desai, col. 4, lines 9-15)

> There are different types of planarization processes which may be utilized in the present invention. The first planarization process is an acid planarization process, in which materials which are highly reactive to acid attack (which are directly exposed to the first planarization process) are removed at a higher rate than materials which are less reactive to acid attack. The second planarization process, which occurs subsequent to the first planarization process in the present invention, is a base planarization process. The second planarization process involves application of bases (for example, alkalis) to the upper surface 42 of the semiconductor chip 18, to remove materials which are highly reactive to attack from bases and at a faster rate than materials which are less reactive to bases. It is generally known what the rate of removal of each of the materials are when they are attacked from each of the first and second planarization processes. Therefore, it can also be determined how much time each of the planarization processes is to be applied, as well as how thick to make the sacrificial layer.

(Desai col. 4, lines 20-38)

> The first planarization process is continued until the amount of the metallic layer 20 which remains barely covers the connecting stud 24. The connecting stud is typically formed of a tungsten alloy, and as such is highly reactive to attack from the first (acid) planarization process. However, the connecting stud does not react strongly to the application of the second (base) planarization process. Therefore, it is important to time the duration of the first planarization process such that the connecting stud 24 will be covered during the entire process.

(Desai, col. 5, lines 6-15)

Applicants have amended claim 14 to include the limitation of chemical mechanical polish. Claim 16 has been cancelled. Applicants respectfully submit that the limitation of chemical mechanical polish to create an ILD recess, as claimed, is not disclosed in Desai.

A closer reading of Desai shows that Desai is concerned with the removal of a metallic layer while leaving a foundation (which includes the ILD) intact.

A closer reading of Desai reveals that the sacrificial layer cited by the Examiner is not the ILD layer (though formed of a similar material). The sacrificial layer is placed over the ILD layer and "configured such that the planarization processes will remove material from the sacrificial layer instead of the dielectric layer." This clearly shows the intent of Desai, which is to protect the ILD.

The statement cited by the Examiner that the sacrificial layer has a relatively slow removal rate for the first planarization process and a relatively high removal rate for the second planarization process is more fully explained and qualified elsewhere in Desai.

> "Even though the sacrificial layer 40 is attacked by both the first planarization process and the second planarization process, the rate at which the material of the sacrificial layer 40 is removed by both of the planarization processes is relatively slow compared to the rate at which the metallic layer 20 is removed."

(Desai, col. 4, lines 57 – 63)

The planarization processes of Desai could not be used to create an ILD recess as claimed, because each of the planarization processes disclosed attack the metallic layer more vigorously than the ILD.

For these reasons, applicants respectfully submit that amended claim 14 is not rendered obvious by Gupta in view of Barth and Forouhi and further in view of Desai. Given that claims 15, 17, 19 and 20 depend from claim 14, it is respectfully submitted that claims 15, 17, 19 and 20 are, likewise, not rendered obvious by Gupta in view of Barth and Forouhi and further in view of Desai.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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